REMARKS

Claims 4 and 5 have been amended. Claims 1-5 are currently pending in the application.

The Examiner rejected claims 1-5 under 35 USC § 102(b) as being anticipated by Miller (USPN 5,027,330). The rejection is respectfully traversed and Applicant requests reconsideration of the application.

In order for a reference to anticipate an invention, each and every element of the claimed invention must be found in a single reference. "Moreover, it is incumbent upon the examiner to identify wherein each and every facet of the claimed invention is disclosed in the applied reference." Ex parte Levy, 17 USPQ2d 1461, 1462 (Bd Pat App & Inter 1990). "The identical invention must be shown in as complete detail as is contained in the ... claim." MPEP § 2131. Applicant respectfully submits that Miller does not anticipate Applicant's claimed invention because Miller does not teach or disclose each and every element of the claimed invention.

Independent claim 4 recites, in relevant part, "a comparator for preventing the at least one processor for writing and the at least another processor for reading from accessing an identical respective one of the plurality of memory circuits simultaneously". Nothing found in Miller teaches the prevention of simultaneous accessing of the same memory circuit. Consequently, for at least this reason, Miller does not anticipate claim 4.

Independent claim 1 recites, in relevant part, "a master controller for setting up the plurality of memory circuits of said memory system using *control commands*

associated with a set of input data and a set of output data". Independent claim 5 includes a limitation similar to the above- italicized language. Nothing found in Miller teaches the use of control commands that are associated with a set of input data and a set of output data.

The Examiner states the "reset circuit 215 and flag circuit 210 represent the 'master controller' of claim 1" (see paragraph 2 of the office action). The signals from the reset and flag circuits, however, are not associated with a set of input data and/or a set of output data. Instead, as shown in figure 2 in Miller, the signal from the reset circuit is associated with the write pointer 235, the read pointer 245, and the flip flop 240. Furthermore, Miller states the input processor (5) "may be arranged to generate on lead 8 a reset signal operative for resetting the ... pointers and other circuitry contained in FIFO 10. Such a reset signal may be generated as a result of, for example, a so-called initialization sequence" (col. 2, lines 49-54).

The signals from flag circuit 210 are also not associated with input and/or output data. The signals from flag circuit 210 are associated with the memory, and are used as flags to indicate the memory is empty (E), half full (HF), and full (F). Miller states the "... flags are generated as a function of the contents of the read and write pointer registers ..." (col. 2, lines 55-62). Thus, reset circuit 215 and flag circuit 210 do not teach "a master controller for setting up the plurality of memory circuits of said memory system using *control commands associated with a set of input data and a set of output data*". For at least this reason, Miller does not anticipate independent claims 1 and 5.

"Claims in dependent form shall be construed to incorporate by reference all the limitations of the claim incorporated by reference into the dependent claim." 37 CFR

1.75. Claims 2 and 3 depend from independent claim 1. Consequently, Miller does not anticipate dependent claims 2 and 3.

In light of the discussion above, Applicant believes that all claims currently remaining in the application are allowable over the prior art and respectfully requests the allowance of such claims.

Respectfully submitted,

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